DATA SHEET

TDA9177
YUV transient improvement processor

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

YUV transient improvement processor TDA9177

FEATURES

- Can be used in $1f_H$ and $2f_H$ applications
- Luminance step improvement
- Line width control
- Smart peaking for detail enhancement
- Embedded feature reduction facility for smart noise control
- Compensating chrominance delay
- YUV interface
- Two additional pins for access to 6-bit ADC and I²C-bus
- Versatile I²C-bus and pin control for user adjustments.

GENERAL DESCRIPTION

The TDA9177 is an I²C-bus controlled sharpness improvement IC with additional inputs for 6-bit analog-to-digital conversion to facilitate additional parameter measurement (e.g. ambient light control). It should preferably be used in front of an RGB video signal processor with YUV interface.

In combination with the TDA9170A, it builds a high performance and intelligent picture improvement solution.

The sharpness processor provides 1D luminance step improvement and detail enhancement by smart peaking, suitable for both $1f_H$ and $2f_H$ applications. The TDA9177 can be used as a cost effective alternative to (but also in combination with) Scan Velocity Modulation (SVM).

An on-board 6-bit Analog-to-Digital Converter (ADC) can be used for interfacing two analog, low frequency voltage signals to the I²C-bus.

The supply voltage is 8 V. The TDA9177 is mounted in a 24-pin SDIP envelope.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		7.2	8.0	8.8	V
$V_{i(Y)}$	luminance input voltage	AMS = LOW	–	0.315	0.42	V
		AMS = HIGH	–	1.0	1.33	V
$V_{i(UV)}$	UV input voltage		–	–	1.9	V
$V_{FS(ADC)}$	full scale ADC input voltage		–	$0.5V_{ref}$	–	V
V_{ref}	reference voltage		3.90	4.00	4.10	V

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9177	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1

BLOCK DIAGRAM

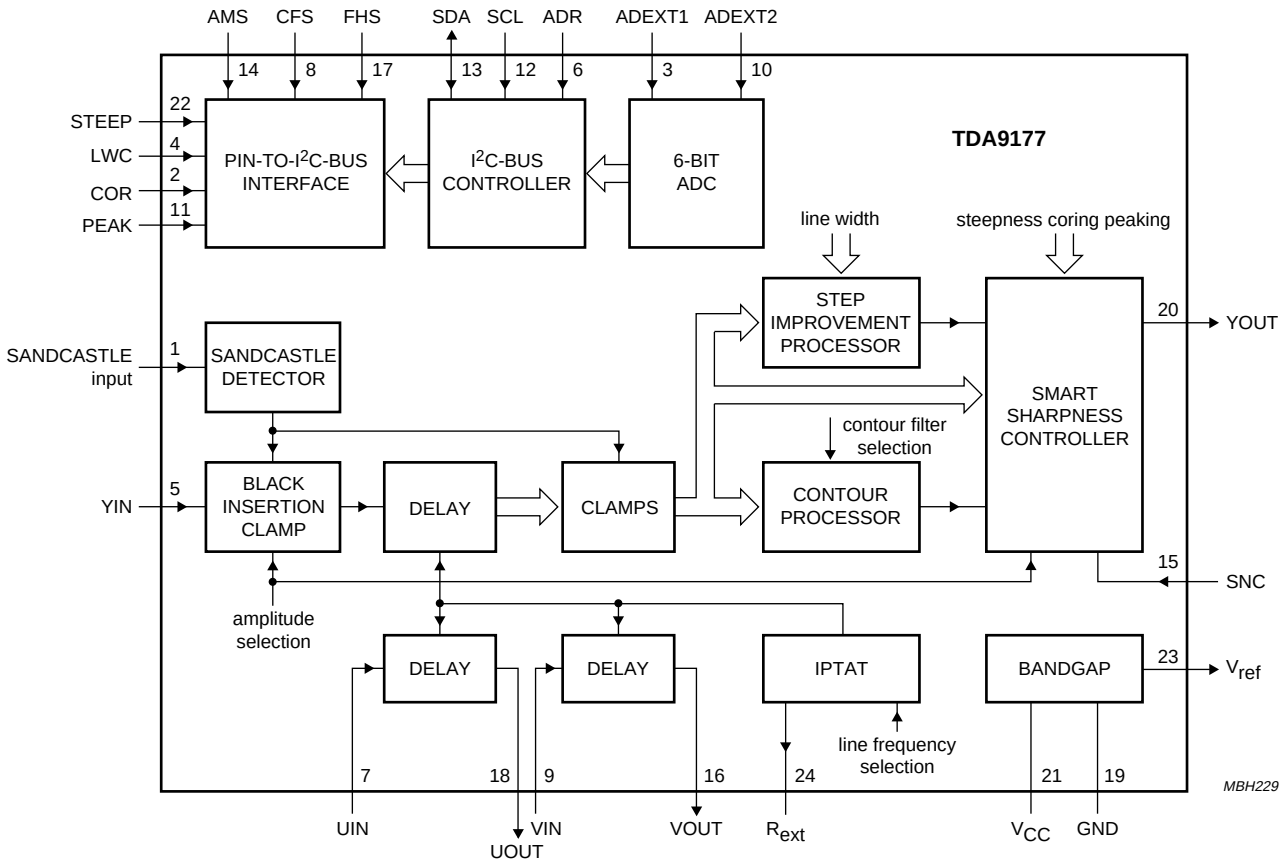


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SANDCASTLE	1	sandcastle input
COR	2	coring level input
ADEXT1	3	ADC input 1
LWC	4	line width control input
YIN	5	luminance input
ADR	6	I^2C-bus address input
UIN	7	colour U input
CFS	8	contour filter select input
VIN	9	colour V input
ADEXT2	10	ADC input 2
PEAK	11	peaking amplitude input
SCL	12	serial clock input (I^2C-bus)
SDA	13	serial data input/output (I^2C-bus)
AMS	14	amplitude select input
SNC	15	smart noise control input
VOUT	16	colour V output
FHS	17	line frequency select input
UOUT	18	colour U output
GND	19	system ground
YOUT	20	luminance output
V_{CC}	21	supply voltage
STEEP	22	steepness control input
V_{ref}	23	reference voltage output
R_{ext}	24	resistor reference

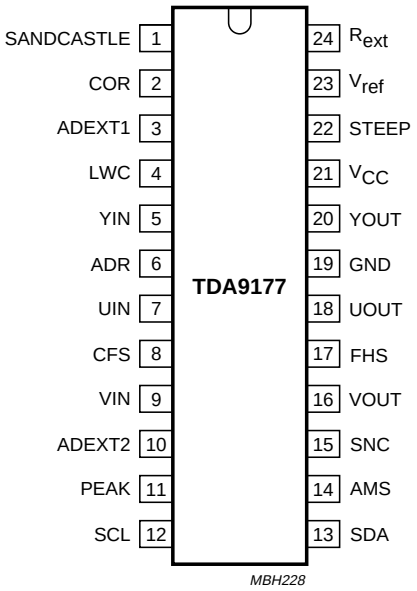


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Y-input selection and amplification

The dynamic range of the luminance input amplifier and output amplifier can be switched between 0.315 V and 1.0 V typically (excluding sync), either externally (pin AMS) or by I²C-bus (bit AMS of the control register). Amplitudes outside the corresponding maximum specified range will be clipped smoothly. The sync part is processed transparently to the output, independently of the feature settings. The input is clamped during the HIGH period of the CLP, defined by the sandcastle reference, and should be DC-decoupled with an external capacitor. During the clamp pulse, an artificial black level is inserted in the input signal to correctly preset the internal circuitry.

The input amplifier drives a delay line of four delay sections, which form the core of the sharpness improvement processor.

Sharpness improvement processor

The sharpness improvement processor increases the slope of large luminance transients of vertical objects and enhances transients of details in natural scenes by contour correction. It comprises three main processing units, these being the step improvement processor, the contour processor and the smart sharpness controller.

STEP IMPROVEMENT PROCESSOR

The step improvement processor (see Fig.9) comprises two main functions:

1. the MINMAX generator
2. the MINMAX fader.

The MINMAX generator utilizes 5 taps of an embedded luminance delay line to calculate the minimum and maximum envelope of all signals momentarily stored in the delay line. The MINMAX fader chooses between the minimum and maximum envelopes, depending on the polarity of a decision signal derived from the contour processor. Figures 4, 5 and 6 show some waveforms of the step improvement processor and illustrate that fast transients result with this algorithm. The MINMAX generator also outputs a signal that represents the momentary envelope of the luminance input signal. This envelope information is used by the smart sharpness controller.

Limited line width control (also called aperture control) can be performed externally (pin 4, LWC) or by I²C-bus (LW-DAC). Line width control can be used to compensate for horizontal geometry because of the gamma or blooming of the spot of the CRT.

THE CONTOUR PROCESSOR

The contour processor comprises two contour generators with different frequency characteristics. The contour generator generates a second-order derivative of the incoming luminance signal and is used both as a decision signal for the step improvement processor and as a luminance correction signal for the smart sharpness controller. In the smart sharpness controller, this correction signal is added to the proper delayed original luminance input signal, making up the peaking signal for detail enhancement. The peaking path is allowed to select either the narrow- or wide-peaked contour generators either externally (pin 8, CFS) or by I²C-bus (bit CFS in the control register). The step improvement circuitry always selects the wide-peaked contour filter.

The contour generators utilize 3 taps (narrow band) or 5 taps (broad band) of the embedded luminance delay lines. Figures 11 and 12 illustrate the normalized frequency transfer of both the narrow and wide contour filters.

SMART SHARPNESS CONTROLLER

The smart sharpness controller (see Fig.10) is a fader circuit that fades between peaked luminance and step-improved luminance, defined by the output of a step discriminating device known as the step detector. It also contains a variable coring level stage.

The step detector behaves like a band-pass filter, so both amplitude of the step and its slope add to the detection criterion. The smart sharpness controller has four user controls:

1. Steepness control
2. Peaking control
3. Coring level control
4. Smart Noise control.

Control settings can be performed either by the I²C-bus or externally by pin, depending on the status of the I²C-bus bit STB.

The steepness setting controls the amount of steepness in the edge-correction processing path. The peaking setting controls the amount of contour correction for proper detail enhancement.

The envelope signal generated by the step improvement processor modulates the peaking setting in order to reduce the amount of peaking for large sine excursions.

The coring setting controls the coring level in the peaking path for rejection of high-frequency noise. All three settings facilitate reduction of the impact of the sharpness features, e.g. for noisy luminance signals.

An external noise detector and a user-preferred noise algorithm are needed to make a fully automatic I²C-bus controlled smart sharpness control.

An on-board, hard-wired smart sharpness algorithm can be executed by driving pin SNC with the output of an external noise detector. This pin, however, is active both in I²C-bus and pin mode. Figures 13 and 14 illustrate the impact of the noise control voltage at pin SNC on the user settings.

Figure 15 shows the relationship between the feature settings STEEP, COR, PEAK, LWC and their corresponding pin voltages.

Chrominance compensation

The chrominance delay lines compensate for the delay of the luminance signal in the step improvement processor, to ensure a correct colour fit. No delay compensation will be performed in the chrominance path for line-width corrections in the luminance path.

Successive approximation ADC

Pins ADEXT1 and ADEXT2 are connected to a 6-bit successive approximation ADC, via a multiplexer. The multiplexer toggles between the inputs with each field.

For each field flyback, a conversion is started for either of the two inputs and the result is stored in the corresponding bus register, ADEXT1 or ADEXT2.

In this way, any analog, slowly varying signal can be given access to the I²C-bus. If a register access conflict occurs, the data of that register is made invalid by setting the flag bit DV (Data Valid) to zero.

I²C-bus

At power up, the bit STB (standby) in the control register is reset, to leave control to the pins. However, the I²C-bus is at standby and responds if properly addressed. By setting STB to logic 1, the control of all features is instead left to the I²C-bus registers. The PDD bit (Power Down Detected) in the status register is set each time an interruption of the supply power occurs and is reset only by reading the status register. A 3-bit identification code can also be read from the status register, which can be used to automatically configure the application by software.

The input control registers can be written sequentially by the I²C-bus by the embedded automatic subaddress increment feature or by addressing it directly. The output control functions cannot be addressed separately. Reading out the output control functions always starts at subaddress 00 and all subsequent words are read out by the automatic subaddress increment procedure. The I²C address is 40H if pin 6 (ADR) is connected to ground and E0H if pin 6 (ADR) is connected to pin 23 (V_{ref}).

I²C-bus specification

Slave address

A6	A5	A4	A3	A2	A1	A0	R/W
ADR	1	ADR	0	0	0	0	X

Auto-increment mode available for subaddresses.

Control functions

FUNCTIONS	TYPE	SUBADDRESS	DATA BYTE							
			D7	D6	D5	D4	D3	D2	D1	D0
Inputs										
Control	REG	00	X	X	X	X	CFS	FHS	AMS	STB
Peaking	DAC	01	X	X	PK5	PK4	PK3	PK2	PK1	PK0
Steepness	DAC	02	X	X	SP5	SP4	SP3	SP2	SP1	SP0
Coring	DAC	03	X	X	CR5	CR4	CR3	CR2	CR1	CR0
Line width	DAC	04	X	X	LW5	LW4	LW3	LW2	LW1	LW0
Outputs										
Status	REG	00	0	0	0	0	ID2	ID1	ID0	PDD
ADEXT1 (output)	REG	01	0	DV	AD5	AD4	AD3	AD2	AD1	AD0
ADEXT2 (output)	REG	02	0	DV	AD5	AD4	AD3	AD2	AD1	AD0

INPUT SIGNALS

Table 1 Address selection

ADR	FUNCTION
0	I^2C address is 40H
1	I^2C address is E0H

Table 2 Standby

STB	FUNCTION
0	pin mode
1	I^2C-bus mode

Table 3 Amplitude selection

AMS	FUNCTION
0	0.315 V luminance
1	1.0 V luminance

Table 4 Line frequency selection

FHS	FUNCTION
0	$1f_H$
1	$2f_H$

Table 5 Contour filter selection

CFS	FUNCTION
0	narrow contour filter
1	wide contour filter

Table 6 Peaking amplitude

PK5 to PK0	FUNCTION
000000	0%
111111	100%

Table 7 Steepness correction

SP5 to SP0	FUNCTION
000000	0%
111111	100%

Table 8 Coring level

CR5 to CR0	FUNCTION
000000	0%
111111	100%

Table 9 Line width correction

LW5 to LW0	FUNCTION
000000	0%
111111	100%

OUTPUT SIGNALS

Table 10 Power Down Detection (PDD)

PDD	FUNCTION
0	no power down detected since last read action
1	power down detected

Table 11 Identification (version number or derivative type)

ID2 to ID0	FUNCTION
000	TDA9177/N1

Table 12 Data valid of ADC registers

DV	FUNCTION
0	data not valid because of possible register access collision
1	data valid

Table 13 Bits AD5 to AD0

AD5 to AD0	FUNCTION
000000B	0 V
111111B	$0.5V_{ref}$

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+8.8	V
V_i	input voltage on any input		–0.5	$V_{CC} + 0.5$	V
V_o	output voltage of any output		–0.5	$V_{CC} + 0.5$	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–10	+70	°C

QUALITY SPECIFICATION

Quality level in accordance with *“SNW-FQ-611 part E”*. The numbers of the quality specification can be found in the *“Quality reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

All pins are protected against ESD by means of internal clamping diodes. The protection circuit meets the specification:

Human body model (100 pF,1500 Ω): All pins >3000 V.

Machine model (200 pF, 0 Ω): All pins >300 V.

Latch-up:

At an ambient temperature of 70 °C, all pins meet the specification:

$I_{trigger} > 100$ mA or $V_{pin} > 1.5V_{CC(max)}$

$I_{trigger} < -100$ mA or $V_{pin} < -0.5V_{CC(max)}$

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	<59	K/W

CHARACTERISTICS

V_{CC} = 8 V; R_{ref} = 10 kΩ ±2%; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
MAIN SUPPLY V_{CC} (PIN 21)						
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	$1f_H$ mode	–	40	–	mA
		$2f_H$ mode	–	45	–	mA
REFERENCE SUPPLY V_{ref} (PIN 23)						
V_{ref}	reference supply voltage		3.90	4.00	4.10	V
$I_{L(max)}$	maximum load current		1.0	–	–	mA
RESISTOR REFERENCE R_{ext} (PIN 24)						
V_{Rref}	resistor supply voltage		–	2	–	V
R_{ref}	resistor value		–	10	–	kΩ
Luminance input/output selection						
LUMINANCE INPUT YIN (PIN 5)						
$V_{i(Y)}$	luminance input voltage	AMS = LOW	–	0.315	0.42	V
		AMS = HIGH	–	1.0	1.33	V
$V_{i(Yclamp)}$	luminance input voltage level during clamping		–	4.0	–	V
$I_{ib(Y)}$	luminance input bias current	no clamp	–	–	0.1	µA
LUMINANCE INPUT VOLTAGE RANGE SELECTION AMS (PIN 14); note 1						
V_{AMSL}	input voltage for low luminance range		–	–	0.5	V
V_{AMSH}	input voltage for high luminance range		3.5	–	5.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LUMINANCE OUTPUT YOUT (PIN 20)						
$V_{o(Y)\ (p-p)}$	luminance output voltage, peak-to-peak	AMS = LOW	–	0.315	–	V
		AMS = HIGH	–	1.0	–	V
$V_{o(Yclamp)}$	luminance output voltage during clamping	AMS = LOW	–	2.35	–	V
		AMS = HIGH	–	2	–	V
S/N(Y)	luminance output signal-to-noise ratio		52	–	–	dB
B_Y	luminance bandwidth	$1f_H$ mode (–1 dB); transparent	5	–	–	MHz
		$2f_H$ mode (–1 dB); transparent	10	–	–	MHz
E_{bl}	black level error	transparent	–	0	1.0	%
$E_{G(n)}$	nominal gain error	transparent	–	0	5	%
R_{out}	output resistance		–	–	150	Ω
I_{ob}	output bias current		1.3	–	–	mA
Step improvement						
GENERAL						
$t_{r(min)}$	minimum rise time 10% to 90%	$1f_H$ mode; note 2	–	20	–	ns
		$2f_H$ mode; note 2	–	20	–	ns
LINE WIDTH CONTROL						
$\delta_{(min)}$	minimum duty factor	2 MHz	–	33	–	%
$\delta_{(max)}$	maximum duty factor	2 MHz	–	67	–	%
$t_{sd(max)}$	maximum step displacement	$1f_H$ mode	–	140	–	ns
		$2f_H$ mode	–	70	–	ns
LINE-WIDTH CONTROL LWC (PIN 4); note 1						
$V_{i(min)}$	input voltage for minimum line width		–	–	37.5	$\%V_{ref}$
$V_{i(max)}$	input voltage for maximum line width		87.5	–	137.5	$\%V_{ref}$
I_{bias}	input bias current		–	0.5	–	μA
Contour processing						
CONTOUR FILTER NARROW-PEAKED						
f_{pc}	peaking centre frequency	$1f_H$	–	3.57	–	MHz
		$2f_H$	–	7.14	–	MHz
CONTOUR FILTER WIDE-PEAKED						
f_{pc1}	peaking centre frequency	$1f_H$	–	4.14	–	MHz
		$2f_H$	–	8.28	–	MHz
Q_{max}	maximum contour amplitude at centre frequency	note 3	–	12	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CONTOUR FILTER SELECTION CFS (PIN 8); note 1						
$V_{i(ncf)}$	input voltage for narrow contour filter		–	–	0.5	V
$V_{i(wcf)}$	input voltage for wide contour filter		3.5	–	5.5	V
Smart sharpness controller						
STEP DETECTOR						
f_{dc}	detection centre frequency	$1f_H$	–	2.13	–	MHz
		$2f_H$	–	4.26	–	MHz
CORING						
Q_{smcL}	minimum coring level	note 4	–	0	–	%
Q_{smcH}	maximum coring level	note 4	–	22	–	%
CORING LEVEL CONTROL COR (PIN 2); note 1						
$V_{i(min)}$	input voltage for minimum coring		–	–	37.5	$\%V_{ref}$
$V_{i(max)}$	input voltage for maximum coring		87.5	–	137.5	$\%V_{ref}$
I_{bias}	input bias current		–	–	0.5	µA
PEAKING LEVEL CONTROL PEAK (PIN 11); note 1						
$V_{i(min)}$	input voltage for minimum peaking		–	–	37.5	$\%V_{ref}$
$V_{i(max)}$	input voltage for maximum peaking		87.5	–	137.5	$\%V_{ref}$
I_{bias}	input bias current		–	–	0.5	µA
STEEPNESS LEVEL CONTROL STEEP (PIN 22); note 1						
$V_{i(min)}$	input voltage for minimum steepness		–	–	37.5	$\%V_{ref}$
$V_{i(max)}$	input voltage for maximum steepness		87.5	–	137.5	$\%V_{ref}$
I_{bias}	input bias current		–	–	0.5	µA
SMART NOISE CONTROL SNC (PIN 15)						
V_{nfr}	level for no feature reduction		–	0.0	–	V
V_{cfr}	level for complete feature reduction		–	V_{ref}	–	V
I_{bias}	input bias current		–	–	1.0	µA
Overall group delay performance for luminance						
t_d	delay time from input to output	$1f_H$ mode	–	175	–	ns
		$2f_H$ mode	–	108	–	ns
t_{de}	delay error contour correction	$1f_H$ mode; note 5	–	0	10	ns
		$2f_H$ mode; note 5	–	0	5	ns
t_{de1}	delay error step correction	$1f_H$ mode; note 5	–	0	10	ns
t_{de2}	delay error step correction	$2f_H$ mode	–	0	5	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DELAY TIME SELECTION FHS (PIN 17); note 1						
V_{i1fH}	input voltage for $1f_H$		–	–	0.5	V
V_{i2fH}	input voltage for $2f_H$		3.5	–	5.5	V
Colour difference processing						
COLOUR DIFFERENCE INPUTS UIN AND VIN (PINS 7 AND 9)						
$V_{iUIN(p-p)}$	input voltage range UIN, peak-to-peak		1.9	–	–	V
$V_{iVIN(p-p)}$	input voltage range VIN, peak-to-peak		1.9	–	–	V
I_{bias}	input bias current UIN, VIN	no clamp	–	–	0.1	μA
V_{cl}	voltage level during clamping		–	4.0	–	V
COLOUR DIFFERENCE OUTPUTS UOUT AND, VOUT (PINS 18 AND 16)						
$V_{o(cl)}$	output voltage level during clamping		–	3.2	–	V
G	gain		–	1.0	–	
E_{off}	offset error	transparent	–	0	1	%
E_G	gain error	transparent	–	0	5	%
$E_{G(UV)}$	UV gain tracking error	transparent	–	0	1	%
B	bandwidth	$1f_H$	7	–	–	MHz
		$2f_H$	7	–	–	MHz
t_d	delay time	$1f_H$	–	175	–	ns
		$2f_H$	–	108	–	ns
R_{out}	output resistance		–	–	150	Ω
I_{ob}	output bias current		0.5	–	–	mA
Successive Approximation ADC						
ADEXT1 AND ADEXT2 (PINS 3 AND 10)						
V_{FS}	full scale input voltage range	with respect to GND	–	2.0	–	V
I_{ib}	input bias current		–	–	1	μA
	data path		–	6	–	bit
DLE	differential linearity error		–	–	1	LSB
ILE	integral linearity error		–	–	1	LSB
f_{con}	conversion frequency	each channel	–	$0.5f_V$	–	Hz
Q_{adt}	conversion time (video lines)	each channel	–	8	–	lines

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Timing						
SANDCASTLE INPUT SANDCASTLE (PIN 1)						
V_{scbn}	detection level for blank	no clamping	1.25	1.5	1.75	V
V_{scbc}	detection level for blank	with clamping and w.r.t. top level sandcastle pulse	–	–0.6	–	V
t_{scnV}	input blanking width for no V-sync		–	–	15	µs
t_{scV}	input blanking width for V-sync		35	–	–	µs
V_{bkvar}	ripple on sandcastle burst key level		–	–	0.4	V
Overall output group delay performance						
$t_{dm(YUV)}$	delay of matching YUV	$1f_H$	–	0	10	ns
		$2f_H$	–	0	5	ns

Notes

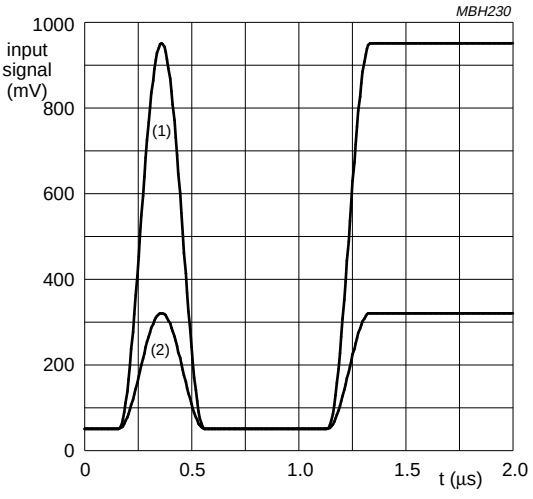
1. This selection is only valid when the standby bit STB is **not** set.
2. Peaking set to minimum. Input signal is a sine wave with the nominal peak-to-peak amplitude corresponding to the selected input range.
3. The contour signal cannot be measured separately from the luminance input signal. The contour signal is also processed by the smart noise controller. The frequency transfer in the peaking mode of the luminance signal can be derived from the frequency transfer of the selected contour signal, taking into account the summation of the contour signal and the luminance input signal. The frequency transfer is most easily measured by sine excitation with a relatively small signal amplitude of 10% of the selected dynamic range of the luminance input, to avoid interaction with the step detector.
4. The coring level refers to the internally selected contour signal. It is dependent on the contour filter selected and is specified for the corresponding peaking centre frequency. The coring level can not be measured explicitly at the luminance output from a big step or sine excitation, because of its interaction with the step detector.
5. Contour correction and step improvement delays are internal delays and cannot be measured in a straightforward way. Contour correction delay mismatch results in asymmetrical ‘ears’ with respect to the centre of the transient. Step improvement correction delay mismatch affects the symmetry of the line width control.

Figures 3 to 8 show the excitation and response of the TDA9177 sharpness improvement processor. The excitation shown in Fig.3 is a 2T-pulse, followed by a step function. Because the TDA9177 can handle both $1f_H$ and $2f_H$ signals, figures illustrating both situations could have been provided. However, as the difference between these two modes (with respect to the TDA9177) is that the time scale of a $2f_H$ response diagram is half that of a $1f_H$ response diagram under equal conditions, only the $1f_H$ figures are shown.

Figure 4 shows that the step improvement processor does not affect small amplitudes. Large transients, however, acquire steeper edges.

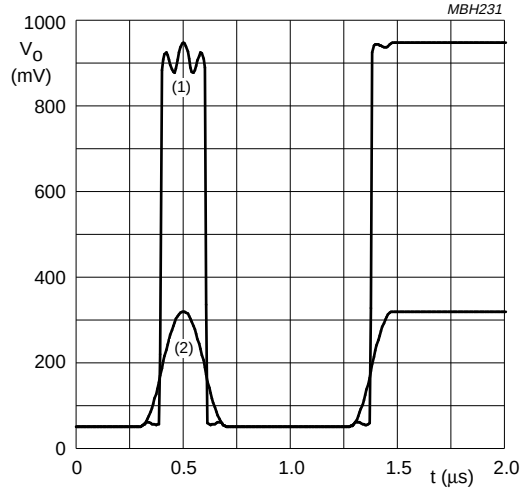
Figures 5 and 6 show that the width of the signal processed by the step improvement processor can be modified by the Line Width Control pin LWC (or DACLW). Figure 7 shows that the contour processor does not affect large transients, but works exclusively on small signals, e.g. details in a video signal.

Figure 8 shows the combination of smart peaking and the step improvement processor; small signals will be affected by the contour processor, while large transients will be modified by the step improvement processor.



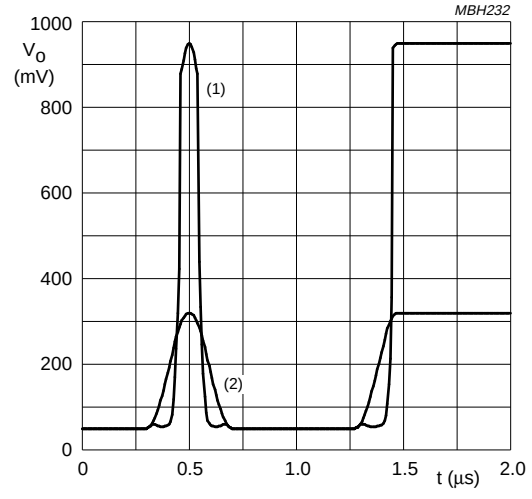
(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.3 Excitation signals: 90% and 30% of nominal amplitude 2T-pulse and step function.



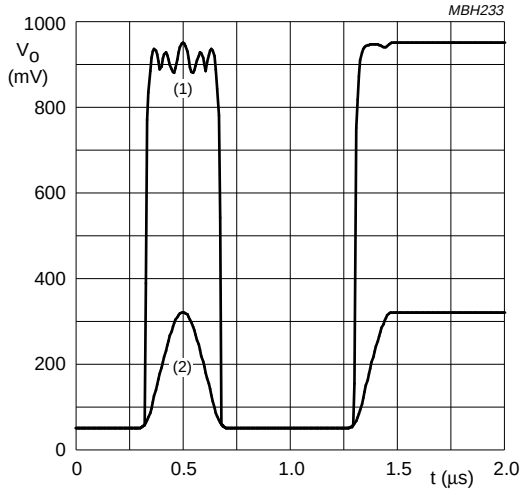
(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.4 Response signals for maximum step improvement, no peaking and nominal line width.



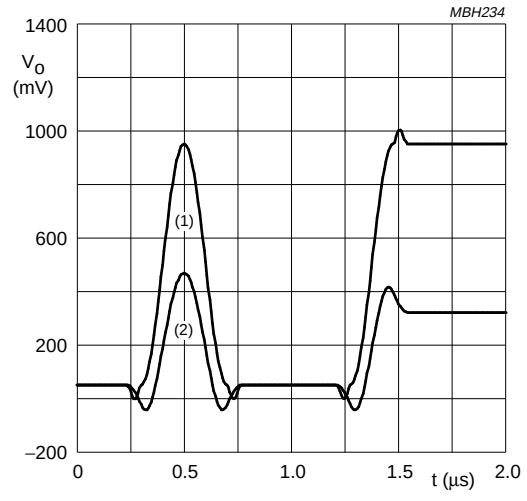
(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.5 Response signals for maximum step improvement, no peaking and minimum line width.



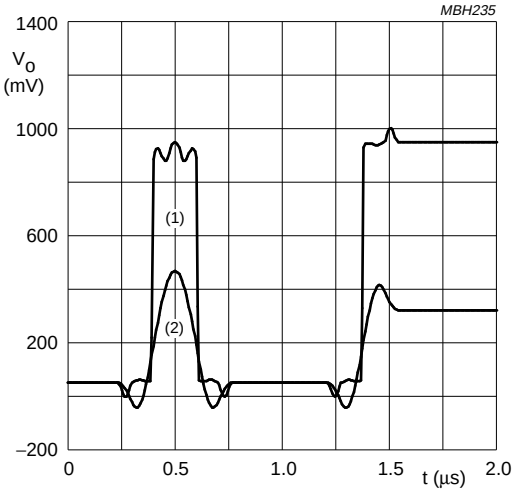
(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.6 Response signals for maximum step improvement, no peaking and maximum line width.



(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.7 Response signals for no step improvement, maximum peaking and 0% coring.



(1) 90% of nominal amplitude.
(2) 30% of nominal amplitude.

Fig.8 Response signals for maximum step improvement, nominal line width, maximum peaking and 0% coring.

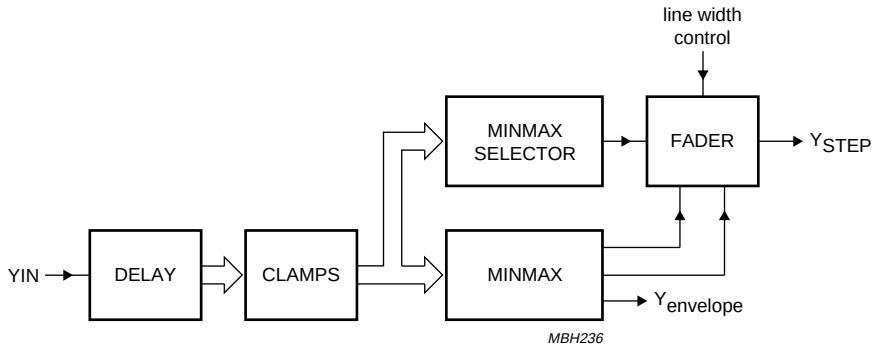


Fig.9 Block diagram of the step improvement processor.

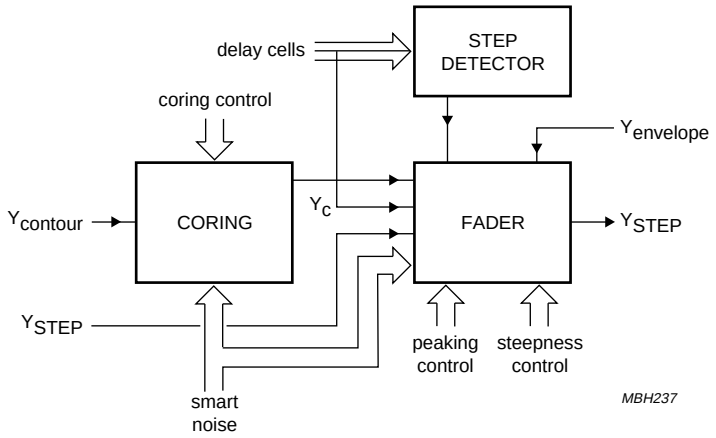
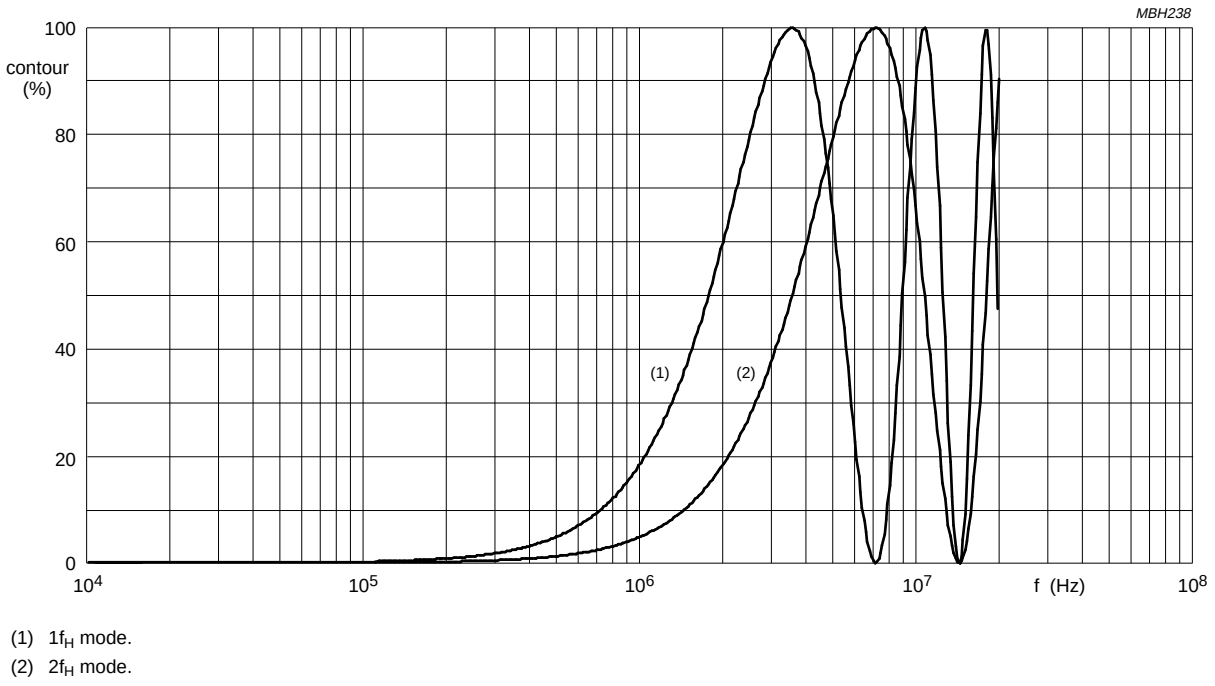
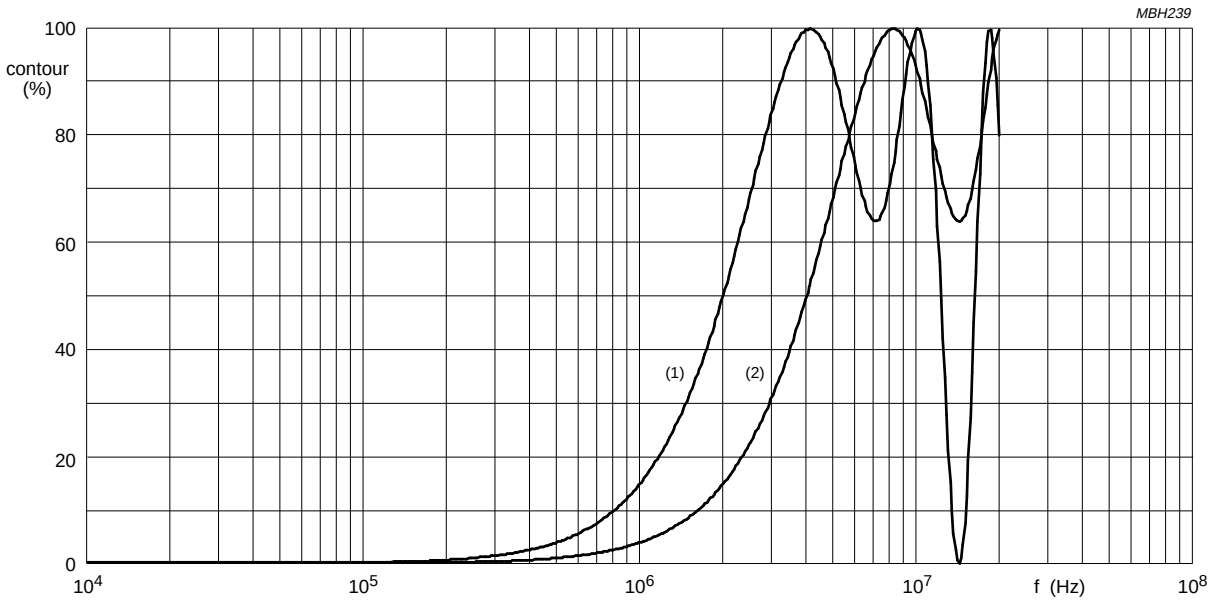


Fig.10 Block diagram of the smart sharpness controller.



(1) $1f_H$ mode.
(2) $2f_H$ mode.

Fig.11 Frequency transfers narrow contour filter.



(1) $1f_H$ mode.
(2) $2f_H$ mode.

Fig.12 Frequency transfers wide contour filter.

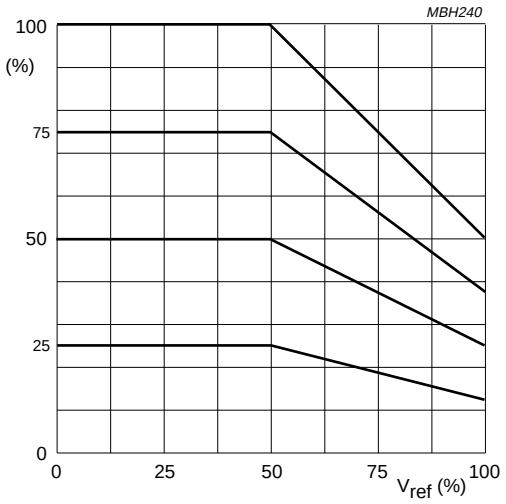


Fig.13 Relative decrease of steepness level as a function of voltage at pin SNC starting from four different steepness level presets.

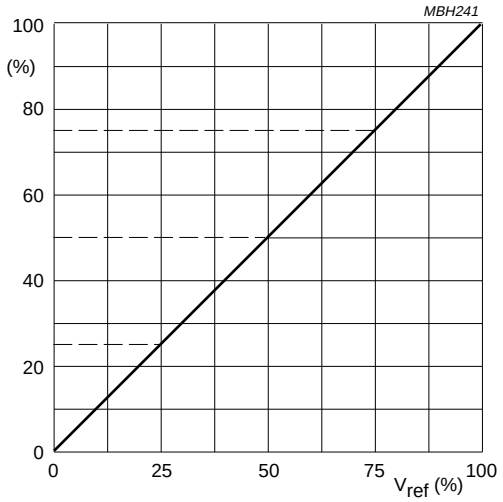


Fig.14 Relative increase of coring level as a function of voltage at pin SNC starting from four different coring level presets.

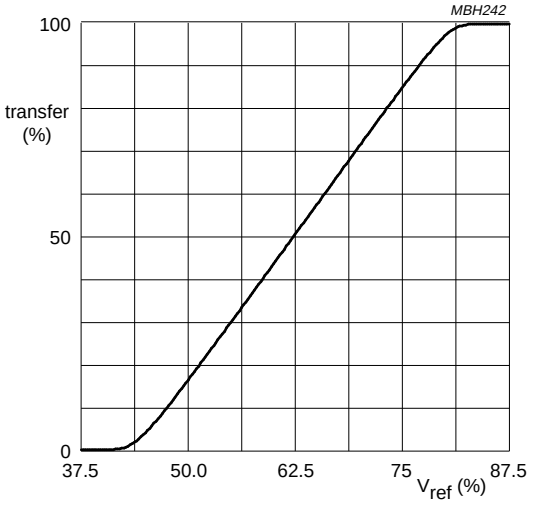


Fig.15 Feature setting control as a function of the pin voltage for peaking, coring, steepness and line width.

INTERNAL CIRCUITRY

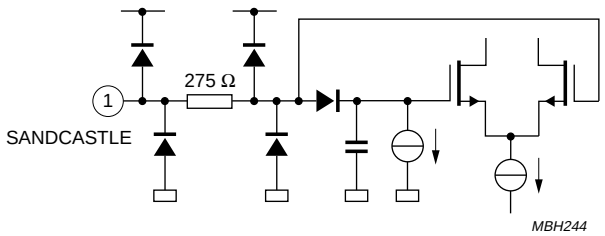


Fig.16 Simplified circuit diagram pin 1.

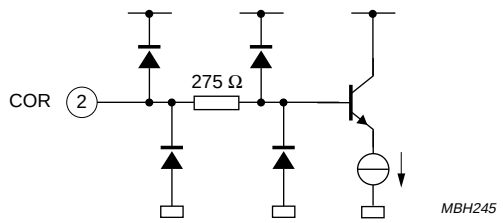


Fig.17 Simplified circuit diagram pin 2.

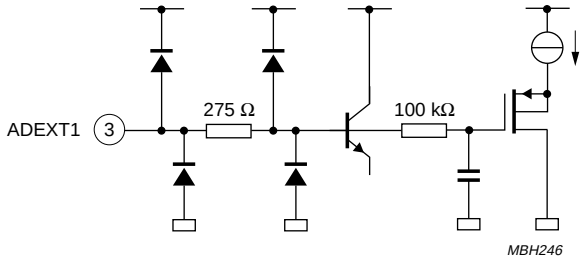


Fig.18 Simplified circuit diagram pin 3.

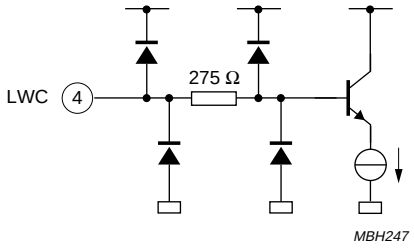


Fig.19 Simplified circuit diagram pin 4.

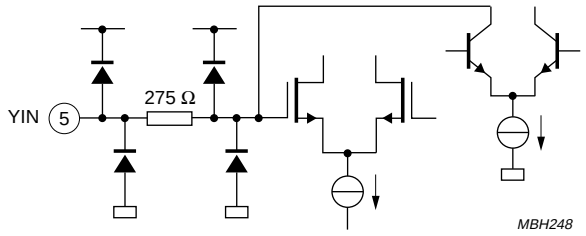


Fig.20 Simplified circuit diagram pin 5.

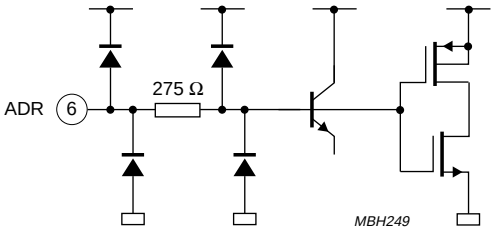


Fig.21 Simplified circuit diagram pin 6.

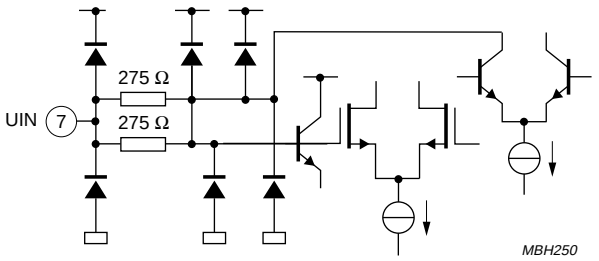


Fig.22 Simplified circuit diagram pin 7.

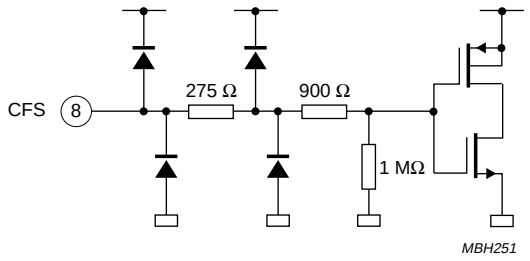


Fig.23 Simplified circuit diagram pin 8.

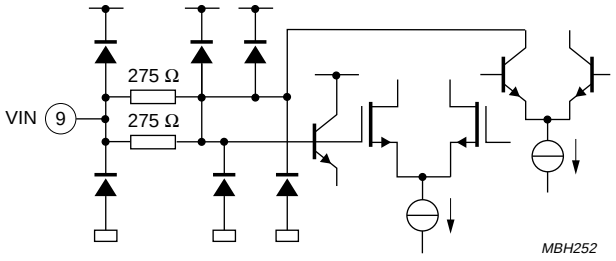


Fig.24 Simplified circuit diagram pin 9.

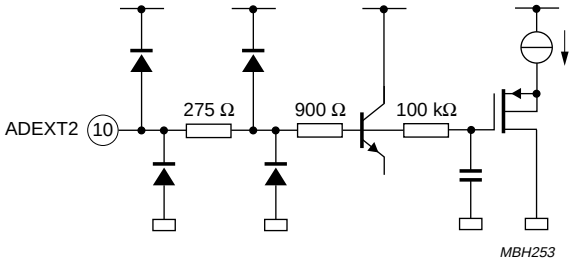


Fig.25 Simplified circuit diagram pin 10.

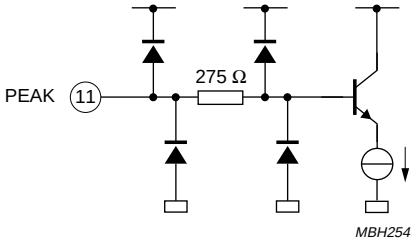


Fig.26 Simplified circuit diagram pin 11.

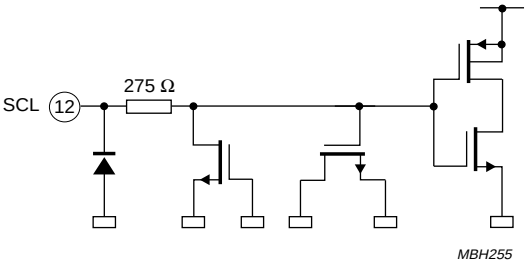


Fig.27 Simplified circuit diagram pin 12.

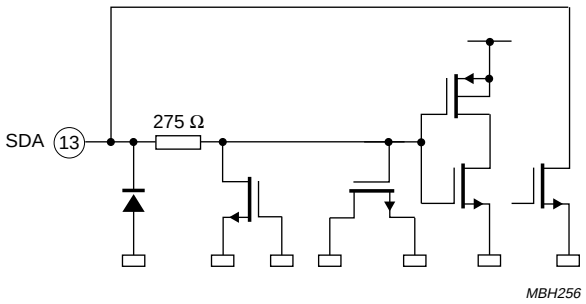


Fig.28 Simplified circuit diagram pin 13.

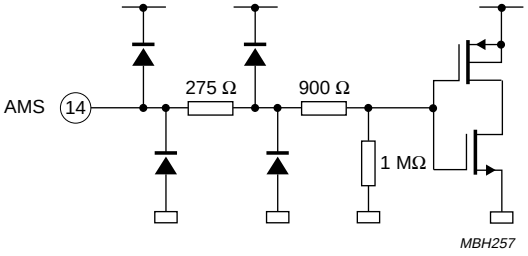


Fig.29 Simplified circuit diagram pin 14.

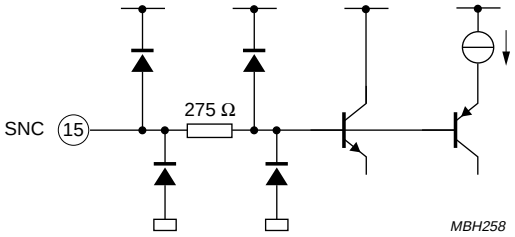


Fig.30 Simplified circuit diagram pin 15.

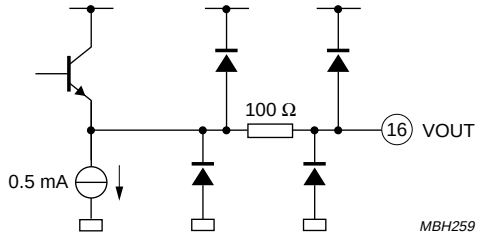


Fig.31 Simplified circuit diagram pin 16.

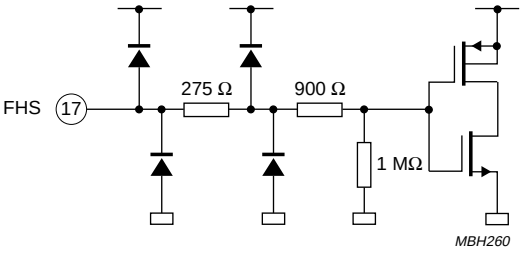


Fig.32 Simplified circuit diagram pin 17.

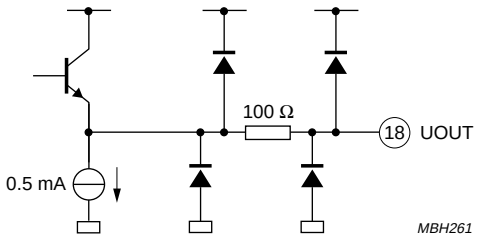


Fig.33 Simplified circuit diagram pin 18.

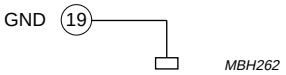


Fig.34 Simplified circuit diagram pin 19.

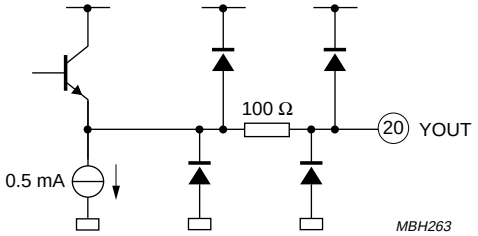


Fig.35 Simplified circuit diagram pin 20.

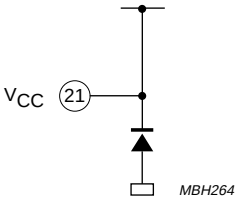


Fig.36 Simplified circuit diagram pin 21.

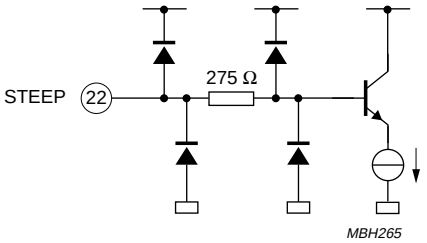


Fig.37 Simplified circuit diagram pin 22.

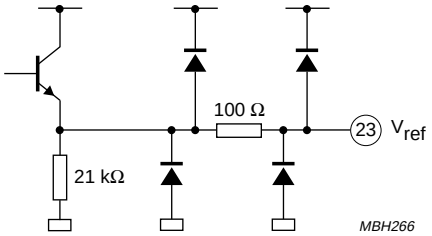


Fig.38 Simplified circuit diagram pin 23.

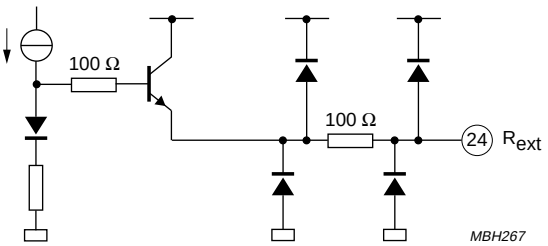


Fig.39 Simplified circuit diagram pin 24.

APPLICATION INFORMATION

The TDA9177 should preferably be used in combination with the TDA9170 or TDA9170A for making a distinct improvement to both contrast and sharpness. To benefit optimally from its picture-sharpening capabilities, the TDA9177 should be positioned as the last part of the YUV-chain.

Feature reduction as a function of the noise contents of the picture can easily be realized in hardware by using the Noise Detector of the TDA9170A. Smart Noise Control (SNC) can be tailor-made for each application, by means of I^{2}C-bus control.

Whenever real-time I^{2}C-bus control is not feasible, the embedded smart sharpness algorithm can be executed by driving pin SNC with the output of the noise detector. In this concept, additional post-processing of the noise detector output can easily be realized with external components.

Figure 40 shows an application example in which the TDA9177 is bus controlled, with the I^{2}C-bus address at 40H. Furthermore, the Smart Noise Control pin (SNC; pin 15) is not used in the example shown.

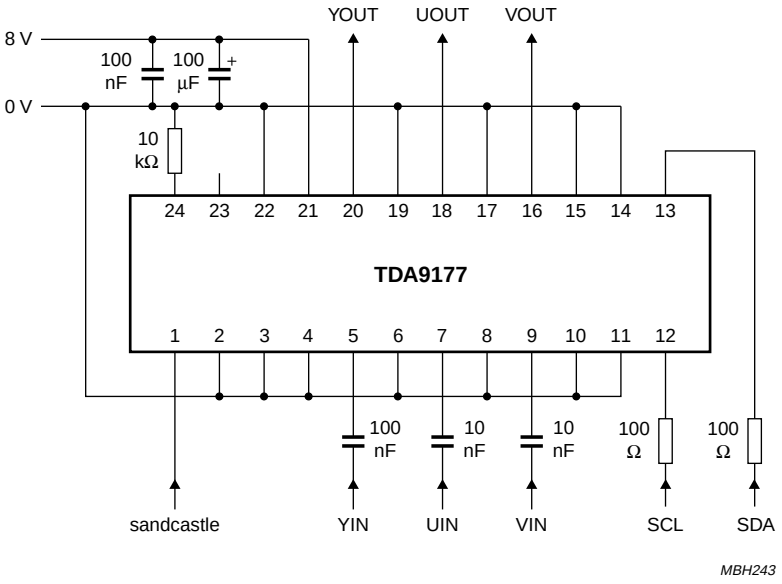
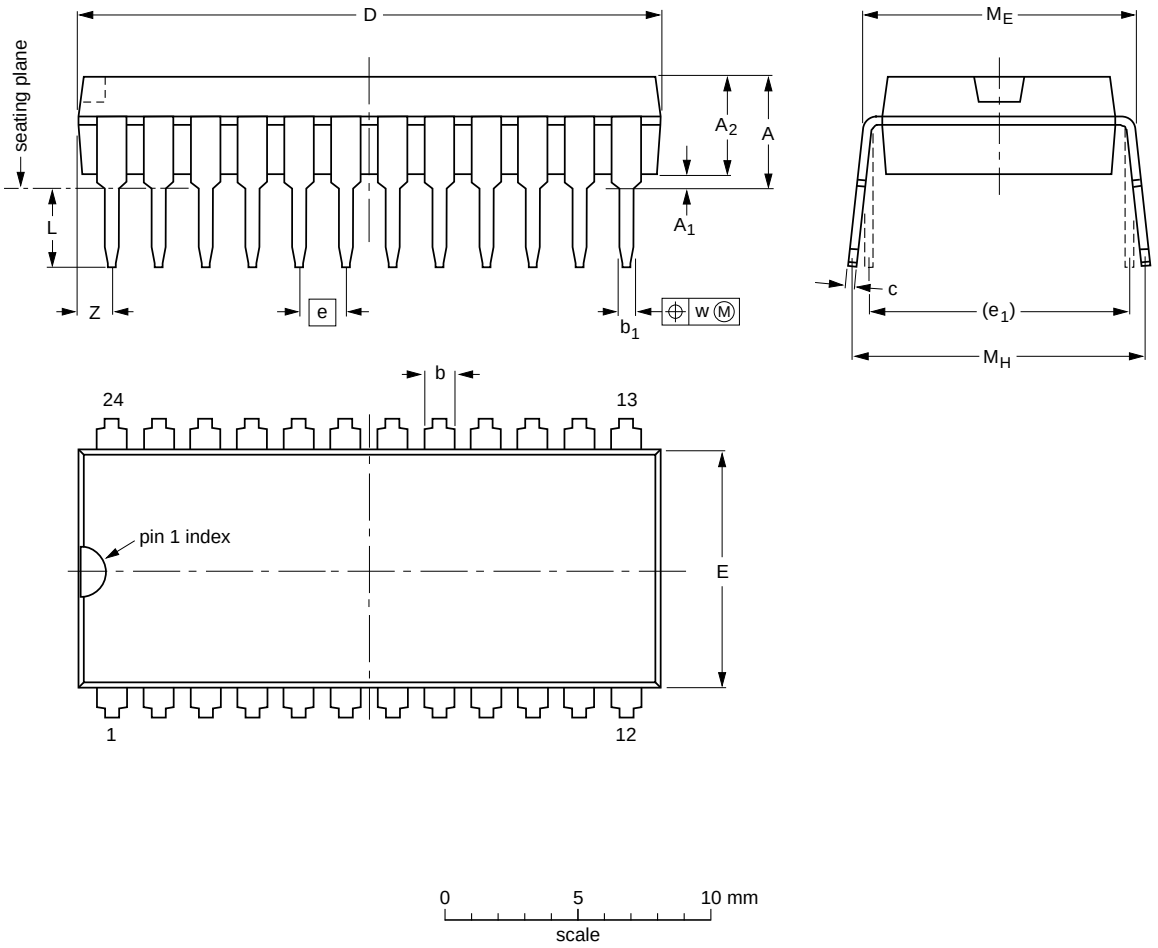


Fig.40 Application diagram.

PACKAGE OUTLINE

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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